COMPUTER MODELING OF MONOLITHIC GaAs IC's

R. L. Van Tuyl, D. Hornbuckle, D. B. Estreich

Hewlett-Packard Company
Santa Rosa Division
Santa Rosa, California

The design of GaAs monolithically integrated circuits in the RF and low microwave frequency range is a process resembling low frequency IC design more than microwave circuit design. These GaAs circuits are directly coupled on-chip in a high-impedance environment. Since tuning and matching elements are not used, the traditional microwave CAD technique of computer optimizing passive element values is not required. Rather, the task of the GaAs IC designer is to predict with computer simulation what the performance of a proposed circuit design will be, then iterate as necessary to achieve the required results.

A complete GaAs IC design may require some, or all, of the following information:

1) DC operating conditions of all circuit elements

2) Transient or switching response

3) Small-signal frequency response

4) Distortion or mixing product analysis of multi-device circuits

5) Circuit noise performance

6) Sensitivity of circuit performance to device parameter variations

7) Circuit performance sensitivity to temperature variation

Three things are required to provide this information:

1) A computer model for the GaAs FET with large-signal non-linear properties which can be linearized for AC analysis

2) A method for computing the parasitic capacitances associated with circuit layout

3) A general purpose circuit simulation program

A general-purpose non-linear device model for the GaAs FET has been developed. This model, which is a two-lump representation of the FET using voltage-dependent current sources and capacitors, describes the non-linear I-V characteristics of the FET (including the gate diode), as well as the principal charge storage elements and their voltage dependences. The GaAs FET model is based on a lumped approximation to the Shockley theory of junction FET's, with the addition of a velocity saturation characteristic necessary to describe the characteristics of the short-channel GaAs FET. Gate-to-channel diode characteristics are described with standard diode equations, and output conductance is modeled empirically. Noise is modeled with empirically derived current sources. The designer can change model input parameters to simulate variation of such process variables as doping density and pinchoff voltage, and to study their effect on circuit response.

Accuracy of frequency response and transient response risetime simulations depends on correct estimation of layout-associated parasitic capacitances. A method for hand calculating parasitic layout capacitances has been developed. Using this method, an analysis of the parasitics associated with a given circuit layout can be performed, and the values inserted as node capacitances into the computer circuit simulation. Circuit metal areas are treated as microstrip sections to determine capacitances to ground, and as coplanar transmission line sections to determine capacitance between features in the plane of the circuit.

Two circuit analysis programs have been used for this work; ASTAP, an IBM product, and HPSPICE, an in-house version of the SPICE program developed at the University of California, Berkeley. Both programs perform DC, transient, and AC analysis. Harmonic distortion and mixing product analysis is accomplished by Fourier analyzing waveforms produced by transient time domain simulation. ASTAP has the advantage of automatic linearization of device models for AC analysis, and complete user freedom in changing the model. This is accomplished at the expense of extra simulation time. HPSPICE requires the device model, including first derivatives of voltage dependent equations, to be stored in advance, and not be accessible to the user. Advantages of the SPICE program include shorter run time, built-in distortion analysis and noise analysis.

Figures 1 through 4 present representative examples of DC, transient, AC, and distortion simulations of GaAs FETs and integrated circuits.

References

1. Van Tuyl, R. L. et al., "GaAs MESFET Logic with 4-GHz Clock Rate," IEEE JOURNAL OF SOLID STATE CIRCUITS, Vol. SC-12, No. 5, Oct. 1977.
2. Van Tuyl, R. L., "A Monolithic Integrated 4 GHz Amplifier," ISSCC DIGEST OF TECHNICAL PAPERS, pp. 72-73; Feb. 1978.
3. Hornbuckle, D., "GaAs IC DC-Coupled Amplifiers," 1980 MICROWAVE SYMPOSIUM DIGEST (this volume).

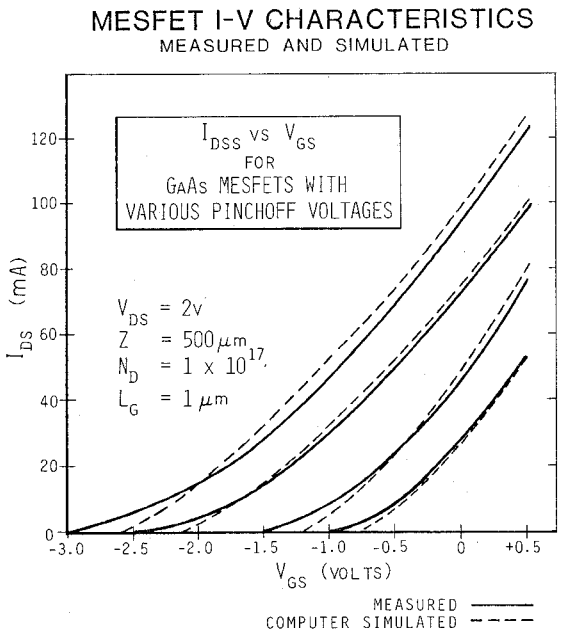

Figure 1. Simulated I_{DS} - vs - V_{GS} compared to measurement for FET's of various pinchoff voltage. Greatest disagreement between simulation and measurement is near pinchoff.

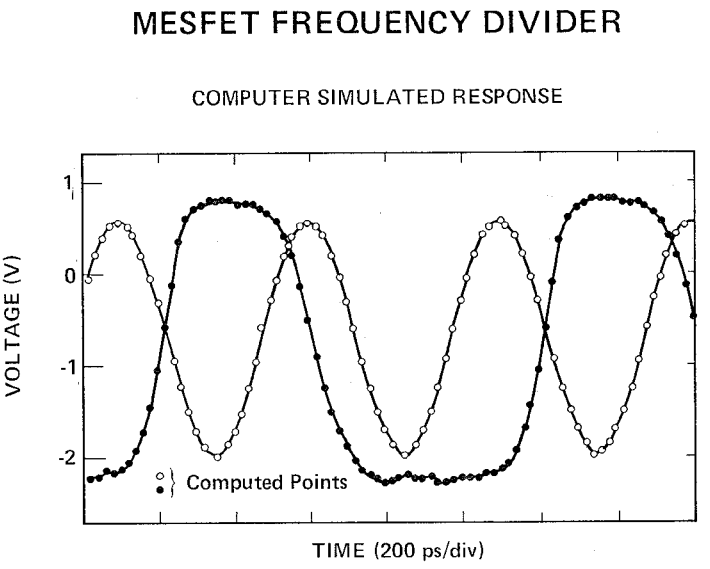

Figure 2. Simulation of a 30-FET binary frequency divider circuit.[1] Input is sinusoidal waveform at 2 GHz, output is asymmetrical square waveform typical of actual circuit operation.

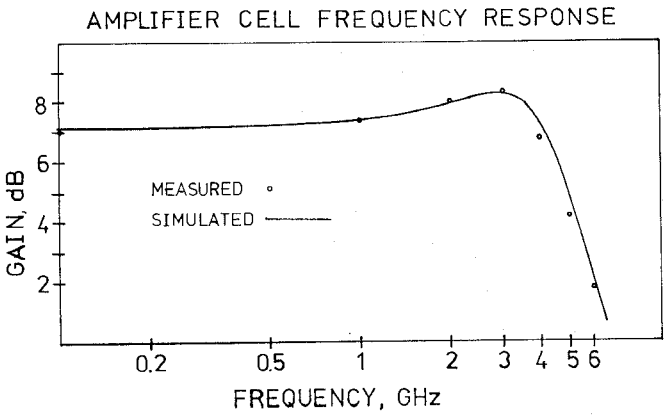

Figure 3. Linear simulation of a feedback amplifier cell's frequency response. (See references 2 and 3 for a discussion of this circuit.) Close agreement of simulation to measurement was obtained by adjusting simulated parasitic capacitances for best fit.

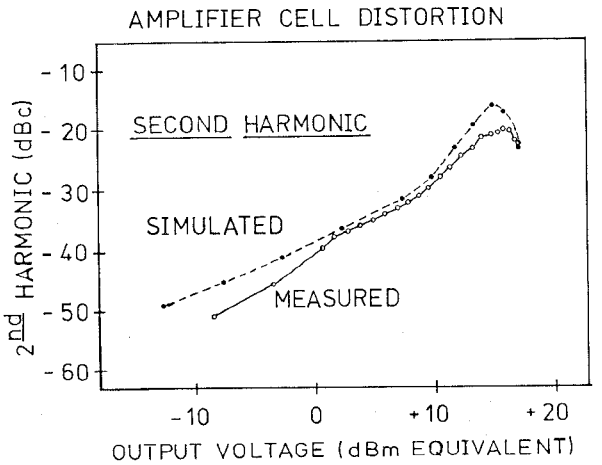

Figure 4. Second harmonic distortion for amplifier cell of Fig. 3. Results were obtained by performing a Fourier analysis on transient simulation output waveform. Note that simulation predicts the decrease of second harmonic at high power level which is actually observed at the onset of symmetrical clipping.